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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Iris Schkilnik

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EXAMINER

HOM, SHICK C

ART UNIT

PAPER NUMBER

2666

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/071,887	Applicant(s) SCHKILNIK ET AL.	
	Examiner Shick C. Horn	Art Unit 2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 February 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-6,8-13,15,18,19,22 and 24 is/are rejected.
- 7) ☒ Claim(s) 3,7,14,16,17,20,21 and 23 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Krishnamoorthy et al. (6,498,798).

Regarding claims 1 and 10:

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Krishnamoorthy et al. disclose a traffic concentrator for combining a plurality of digital data streams into at least one higher speed digital data stream, the traffic concentrator comprising: a plurality of inputs adapted to receive the plurality of digital data streams; a memory having first and second portions; a control circuit, coupled to the plurality of inputs and the memory, the control circuit generating control signals for storing data from the plurality of digital data streams in one of the first and second portions of the memory during a first time slot for retrieval from the portion of the memory during a subsequent time slot for combination and transmission as the at least one higher speed digital data stream (see 2 lines 23-31 which recite the concentrator used to combine multiple lower-speed data streams into a smaller number of higher-speed data streams and the higher-speed data streams are further combined in a multiplexer into one high-speed data stream; col. 1 lines 37-48 which recite buffering to enable several lower speed input ports to share a higher speed output port clearly reads on the memory portions; and col. 3 lines 43-52 which recite the data traffic from the low-speed ports clearly reads on the plurality of inputs adapted to receive the plurality of digital data streams).

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4. Claims 5, 8-9, 15, 18-19 are rejected under 35

U.S.C. 102(b) as being anticipated by Kratz et al. (4,041,461).

Regarding claims 5, 8-9, 15, 18-19:

Kratz et al. disclose a method for bundling a plurality of digital data streams with a first speed to at least one digital data stream with a second, higher speed (in Fig. 1 see the working stores, the storage controller, and bulk store, whereby data streams at 200 nanosecond rate are combined in working store and outputted to the bulk store at a higher speed of 100 nanosecond rate by the storage controller), the method comprising: during even time slots in the plurality of digital data streams: storing data from the plurality of digital data streams in a first memory portion, and reading data from a second memory portion for transmission on the at least one digital data stream with a second, higher speed; and during odd time slots storing data from the plurality of digital data streams in the second memory portion, and reading data from the first memory portion for transmission over the at least one digital data stream with a second, higher speed as in claim 5 and wherein reading data from a second memory portion for transmission on the at least one digital data stream with a second, higher speed comprises: reading the data from the second

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memory portion one time for each of the at least one digital data stream with a second, higher speed; and for each reading of the data from the memory, forming at least one digital data stream with a second, higher speed from a portion of the stored data from the plurality of digital data streams as in claims 8-9 (see col. 46 lines 7-24 which recite the working store WS being organized as two storage elements, allowing simultaneous operation of storing and reading data to and from the AE and STC to the BS).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.

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Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 2, 4, and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamoorthy et al. (6,498,798) in view of Fechalos (4,737,950).

For claims 2, 4, and 11-13 Krishnamoorthy et al. disclose the traffic concentrator described in paragraph 3 of this office action. Krishnamoorthy et al. disclose all the subject matter of the claimed invention with the exception of wherein the memory comprises a dual port, random access memory as in claims 2, 11; wherein the plurality of inputs are adapted to receive at least one of T1 and E1 pulse code modulated (PCM) highways as in claim 4; and wherein the control circuit stores data in one of the first and second portions of each of the plurality of memory devices during mutually exclusive portions of the time slot of the first plurality of digital data streams as in claims 12-13.

Fechalos from the same or similar fields of endeavor teach that it is known to provide memory comprising a dual port,

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random access memory (see Fig. 18 the use of the dual port memory 130 as in claims 2, 11); wherein the plurality of inputs are adapted to receive at least one of T1 and E1 pulse code modulated (PCM) highways (see col. 9 lines 29-35 which recite the use of T1 PCM inputs as in claim 4); and wherein the control circuit stores data in one of the first and second portions of each of the plurality of memory devices during mutually exclusive portions of the time slot of the first plurality of digital data streams (see col. 1 line 62 to col. 2 line 28 which recite controlling the time slots to the memory for channel selection using the multiplexer including the clock means for synchronization clearly reads on storing data in portions of memory during mutually exclusive portions of the time slot as in claims 12-13). Thus, it would have been obvious to the person having ordinary skill in the art at the time the invention was made to use memory comprising a dual port, random access memory; wherein the plurality of inputs are adapted to receive at least one of T1 and E1 pulse code modulated (PCM) highways; and wherein the control circuit stores data in one of the first and second portions of each of the plurality of memory devices during mutually exclusive portions of the time slot of the first plurality of digital data streams as taught by Fechalos in the traffic concentrator of Krishnamoorthy et al. The memory

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comprising a dual port, random access memory; wherein the plurality of inputs are adapted to receive at least one of T1 and E1 pulse code modulated (PCM) highways; and wherein the control circuit stores data in one of the first and second portions of each of the plurality of memory devices during mutually exclusive portions of the time slot of the first plurality of digital data streams can be implemented by replacing the memory comprising a dual port, random access memory; wherein the plurality of inputs are adapted to receive at least one of T1 and E1 pulse code modulated (PCM) highways; and wherein the control circuit stores data in one of the first and second portions of each of the plurality of memory devices during mutually exclusive portions of the time slot of the first plurality of digital data streams of Fechalos for the buffer and lines of Krishnamoorthy et al. The motivation for using the memory comprising a dual port, random access memory; wherein the plurality of inputs are adapted to receive at least one of T1 and E1 pulse code modulated (PCM) highways; and wherein the control circuit stores data in one of the first and second portions of each of the plurality of memory devices during mutually exclusive portions of the time slot of the first plurality of digital data streams as taught by Fechalos in the traffic concentrator of Krishnamoorthy et al. being that it

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provides more efficiency for the concentrator since the concentrator can access the memory at a higher rate using a dual port memory wherein data are stored in one of the first and second portions of each of the plurality of memory devices during mutually exclusive portions of the time slot of the first plurality of digital data streams and data being transferred at a higher rate using T1 and E1 PCM highways.

7. Claims 6, 22, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kratz et al. (4,041,461) in view of Fechalos (4,737,950).

For claims 6, 22, and 24 Kratz et al. disclose the method and traffic concentrator described in paragraph 4 of this office action. Kratz et al. disclose all the subject matter of the claimed invention with the exception of wherein the plurality of inputs are adapted to receive at least one of T1 and E1 pulse code modulated PCM highways as in claim 24; and wherein storing data from the plurality of digital data streams in a first memory portion comprises storing data from a plurality of pulse code modulated PCM highways as in claims 6, 22.

Fechalos from the same or similar fields of endeavor teach that it is known to provide wherein the plurality of inputs are

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adapted to receive at least one of T1 and E1 pulse code modulated (PCM) highways; and wherein storing data from the plurality of digital data streams in a first memory portion comprises storing data from a plurality of pulse code modulated PCM highways (see col. 9 lines 29-35 which recite the use of T1 PCM inputs). Thus, it would have been obvious to the person having ordinary skill in the art at the time the invention was made to use plurality of inputs being adapted to receive at least one of T1 and E1 pulse code modulated (PCM) highways as taught by Fechalos in the method and traffic concentrator of Kratz et al. The plurality of inputs being adapted to receive at least one of T1 and E1 pulse code modulated (PCM) highways can be implemented by replacing the plurality of inputs being adapted to receive at least one of T1 and E1 pulse code modulated (PCM) highways of Fechalos for lines of Kratz et al. The motivation for using the plurality of inputs being adapted to receive at least one of T1 and E1 pulse code modulated (PCM) highways as taught by Fechalos in the method and traffic concentrator of Kratz et al. being that it provides more efficiency and reliability for the method and concentrator since the concentrator can access and transferred data at a higher rate using standard high speed T1 and E1 PCM highways.

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Allowable Subject Matter

8. Claims 3, 7, 14, 16-17, 20-21, and 23 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Saulsbury discloses a method and system for integrating telephone voice communications into a client-server architecture.

Merritt et al. disclose distributed write data drivers for burst access memories.


10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shick C. Hom whose telephone number is 571-272-3173. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH



DANG TON
PRIMARY EXAMINER